PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

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Applicant's or agent's file reference 2003P07186WO					FOR FURTHER	HER ACTION See Form PCT/IPE		See Form PCT/IPEA/416	
Internation	nal app	lication N	о.		International filing	date (day/m	wnth/year)	Priority date (day/month/year)	
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1.					minary examination ne applicant according			International Preliminary Examining Authority	
2.	•							g this cover sheet.	
3.	This re	port is als	ю ассот	panied by A	NNEXES, comprisin	ıg:			
	a. (sent to the applicant and to the International Bureau) a total of 7 sheets, as follows:							sheets, as follows:	
	sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).								
	sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.								
	ь	(sent		nternational	Bureau only) a total	of (indicate	type and number	er of electronic carrier(s))	
					• •			, containing a sequence listing and/or tables	
					r readable form only trative Instructions).	, as indicate	ed in the Supple	emental Box Relating to Sequence Listing (see	
4.	This re	port conta	ains indic	eations relat	ing to the following i	tems:			
	\boxtimes	Box No.	. I	Basis of the	e report				
		Box No.	. II	Priority					
		Box No.	. III	Non-establ	ishment of opinion w	ith regard to	o novelty, invent	tive step and industrial applicability	
		Box No.	. IV	Lack of un	ity of invention				
	Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement						elty, inventive step or industrial applicability;		
	Box No. VI Certain docume			cuments cited	ments cited				
	Box No. VII Certain defects in the international application								
		Box No.	. VIII	Certain ob	servations on the inte	rnational ap	plication		
Date of s	submiss	ion of the	demand			Date of	completion of th	nis report	
Name and mailing address of the IPEA/EP					Authori	Authorized officer			
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Translation

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Box	No. I]	Basis of the report			
1.			the language, this report is based on the internation at this item.	al application in the language in	which it wa	as filed, unless otherwise
		This rep which is	ort is based on translations from the original languag the language of a translation furnished for the purpo	e into the following languageses of:		,
		in	ternational search (Rule 12.3 and 23.1(b))			
		∐ թս	blication of the international application (Rule 12.4)			
			ternational preliminary examination (Rule 55.2 and/o			
2.	recei	iving Offi report):	to the elements of the international application, this to ce in response to an invitation under Article 14 are mational application as originally filed/furnished ription:	eport is based on (replacement s referred to in this report as "o	sheets whic riginally fil	h have been furnished to the led" and are not annexed to
		pages	1,5-8			as originally filed/furnished 2005 with letter
		pages*	2-4,4a	received by this Authority on		03.2005
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	\boxtimes	the clair	ms:			
		nos.			;	as originally filed/furnished
		-				statement) under Article 19
		nos.*	1_12		31.03.	2005 with letter
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3.		The am	tendments have resulted in the cancellation of:			
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4.		This re	port has been established as if (some of) the amendate been considered to go beyond the disclosure as fi	iments annexed to this report an led, as indicated in the Suppleme	u listed bel ental Box (F	ow had not been made, since Rule 70.2(c)).
		<u>Ц</u> :	he description, pages			
		<u> </u>	he claims, nos.			
		L t	he drawings, sheets/figs			
		t	he sequence listing (specify):			
			iny table(s) related to sequence listing (specify):			
*	If it	em 4 app	lies, some or all of those sheets may be marked "sup	erseded."		

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Box	Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement					
1.	Statement		_			
	Novelty ((N) Claims 6, 7, 12, 13	_ YES			
		Claims 1-5, 8-11	_ NO			
	Inventive	e step (IS) Claims	_ YES			
		Claims 1-13	_ NO			
	Industrial	l applicability (IA) Claims 1-13	_ YES			
		Claims Claims	_ NO			
2.	Citations	d explanations (Rule 70.7)				
۷.	1.	This report makes reference to the following				
	±•	documents:				
	D1:	US 4 510 602 A (FORMAZ JEROME ET AL), 9 April 1985				
	= - ·	(1985-04-09)				
	D2:	US 5 623 680 A (MILLS THOMAS L ET AL), 22 April				
	•	1997 (1997-04-22)				
	2.	The present application does not meet the				
		requirements of PCT Article 33(2) because the				
		subject matter of claims 1-5 and 8-11 is not novel				
		over the prior art as defined in the Regulations				
		(PCT Rule 64.1-64.3).				
	2.1	Claim 1:				
		Document D1, which is considered to represent the				
		closest prior art, discloses a control device as				
		defined in claim 1 of the application, having:				
		(a) inputs ("input units 8", column 4, lines 61-				
		68),				
		(b) outputs ("output units 9", column 5, lines 4-				
		16),				

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- (c) a memory unit for storing set values (column 2, lines 50-53, "memories 1, 2", which contain "instructions" and "grid signals". A "set value" corresponds to an "instruction" and its corresponding "grid"), and
- (d) an allocation unit as defined in claim 1 of the application ("comparator 10", "comparison indicator 16", "gate 7, 14", column 3, lines 37-48; column 4, lines 33-55; and column 5, lines 4-
- 46; Column 4, lines 33 33, and column 3, lines 1
- 15. See also the example in column 5, lines 31-
- 47), in which control device
- (e) at least one of the set values can be set in the memory unit with an independence state value
- (D) (value "0" in the "grid memory 2", column 4, lines 32-61); and
- (f) a digital output value can be allocated to one of the digital outputs by means of the allocation unit, independently of the at least one real input value whose associated set value has the independence state value (D) (column 4, lines 32-61);
- (g) the set values having one of the state values 1, 0 or "independence state value" (column 4, 1ines 32-61).

It should be noted that two bits are required to represent a "set value" with three states ("0", "1", "independent"). Consequently, an "instruction" bit which takes the value "0" or "1", forms in D1 a unit with a corresponding "mask" bit which indicates that the input bit is irrelevant. These bits, combined into "words"

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comprising a plurality of inputs", are stored in D1 in parallel in "memory 1" and "memory 2".
"Parallel" means that "memory 1" and "memory 2" are addressed together (column 3, lines 1-3) in such a way that each input set ("instruction", set value) can be invoked and processed together with its corresponding mask word (column 4, lines 40-61; column 5, lines 30-45; claim 1 in D1). D1 uses the term "grid" instead of "mask", but clearly describes the "masking" (column 7, lines 33-45, in D1).

It should also be noted that the term "instruction" with its corresponding "grid" in D1 corresponds to the "set values" of inputs, within the meaning of the present application. This is obvious from column 3, lines 37-41; column 2, line 65 - column 3, line 3; column 4, lines 40-67; column 5, lines 30-45; and column 7, lines 20-25, and also from claim 1 (column 7, lines 45-59 and 60-66) of D1.

The preamble of claim 1, which corresponds to a conventional state automaton, is also disclosed in document D2 (in D2: memory unit is the "RAM 40", where the "application logic table 100" is stored; column 7, lines 32-35; set values: elements in vectors 102, 104,..., 120 in figure 6; column 6, line 12 - column 7, line 20; and column 4, lines 45-50). Furthermore, document D2 discloses (column 6, lines 24-46) the characterising part of claim 1 (in the example depicted in figure 6 of D2,

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"blank", for example in vector "104", corresponds to the independence state value, while vector "102" takes the values "0" or "1").

2.2 Claims 2 and 3:

Document D2 (column 3, line 58 - column 4, line 11) discloses the subject matter of claims 2 and 3. The "A/D converter 52" in D2 corresponds to the "first evaluation unit" in claim 2 of the present application, and to the "logic gates 54" of the "second evaluation unit" in claim 3 of the present application.

2.3 Claim 4:

Document D1 (column 5, lines 28-58) discloses the subject matter of claim 4.

2.4 Claim 5:

Document D2 (figure 5, rows 94 and 96; column 5, line 66 - column 6, line 1; and column 7, lines 7-12) discloses the subject matter of claim 5.

2.5 Claims 8-11:

Claims 8-11 relate to a process whose features correspond to the technical features of the device claims 1-5. In view of the explanations in points 2.1-2.4 above, claims 8-11 are not novel (PCT Article 33(2) and PCT Rule 64.1-64.3).

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3. The present application does not meet the requirement of PCT Article 33(3) because the subject matter of claims 6, 7, 12 and 13 does not involve an inventive step (PCT Rule 65.1, 65.2).

3.1 Claim 6:

Document D2 discloses the subject matter of claims 1-5 but not the additional features of claim 6.

In relation to D2, the problem addressed by the features of the present application can therefore be considered to be that of determining in which circumstances the security state is to be switched on.

The feature which consists in checking whether the real input values deviate for more than a predetermined time from the corresponding set values (claim 6) is only one of several obvious possibilities from which a person skilled in the art would select to solve the stated problem, according to the circumstances, without being inventive. The subject matter of claim 6 therefore does not involve an inventive step (PCT Article 33(3)).

3.2 Claim 7:

The problem addressed by the additional features of claim 7 which have not been disclosed in D2 can

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be considered to be that of checking the integrity of the memory unit.

The checksum feature is a conventional measure. A person skilled in the art would consider the inclusion of this measure in the device described in document D2 an obvious procedure for solving the stated problem. The subject matter of claim 7 therefore does not involve an inventive step (PCT Article 33(3)).

3.3 Claims 12 and 13:

Claims 12 and 13 relate to a process whose features correspond to the technical features of the device claims 6 and 7. In view of the explanations in paragraphs 3.1 and 3.2 above, the subject matter of claims 12 and 13 does not involve an inventive step (PCT Article 33(3)).

4. The application does not meet the requirement of **PCT Article 6** because claims 2 and 9 are unclear. The expression "raw input values" used in claims 2 and 9 is vague and unclear and leaves the reader uncertain about the meaning of the technical feature in question.